

**EXPEDITED PROCEDURE**

**RESPONSE UNDER 37 CFR § 1.116--EXAMINING GROUP 2811**

**PATENT**

|   |  |
|---|--|
| <b>Certificate of Mailing/Transmission (37 C.F.R. § 1.8(a))</b>   |  |
| I hereby certify that this correspondence is, on the date shown below, being:                                     |  |
| ELECTRONIC FILING   | FACSIMILE  |
| <input checked="" type="checkbox"/> transmitted to the United States Patent and Trademark Office's EFS-Web System | <input type="checkbox"/> transmitted by facsimile to the Patent and Trademark Office, (571) 273-8300 |
|   | <u>Arnette Dodge</u><br>Name of Person Certifying  |
| <u>8/9/2006</u><br>Date   | <u>Arnette Dodge</u><br>Signature of Person Transmitting Paper and Fee                               |

**In the United States Patent and Trademark Office**

**Date:** August 9, 2006

**In re Application of:** Gaynes et al.

**Filed:** 11/28/2003

**For:** Optimized Conductive Lid Mounting For Integrated Circuit Chip Carriers

**Serial Number:** 10/707,206

**Art Unit:** 2811

**Examiner:** Junghwa M. Im

**REPLY AND AMENDMENT AFTER FINAL REJECTION UNDER 37 C.F.R. '1.116**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

This is in response to the Final Office Action mailed on June 15, 2006, which is due for response by September 15, 2006. Any fees required in entering this response may be charged to Applicants' deposit account, 09-0456.

Applicants respectfully request reconsideration of the outstanding rejections and reexamination of the present application in light of the following remarks and amendments. No new matter has been included.

FR920030002US1  
SN 10/707,206

## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor package comprising:
  - a chip carrier including a grounded pad on a first side of said chip carrier;
  - a semiconductor chip coupled to said first side of said chip carrier;
  - a conductive lid ~~substantially coplanar with said first side of said chip carrier~~thermally coupled to said semiconductor chip, wherein the entire length of said conductive lid is substantially parallel with said first side of said chip carrier; and
  - a conductive structure electrically coupled to said grounded pad and to said conductive lid.
2. (Original) The semiconductor package of claim 1 wherein a solder connects said conductive structure and said grounded pad.
3. (Original) The semiconductor package according to claim 1 wherein said conductive structure is electrically coupled to said grounded pad with an electrically conductive adhesive material.
4. (Original) The semiconductor package according to claim 1 wherein said conductive structure is electrically coupled to said conductive lid with an electrically conductive adhesive material.
5. (Original) The semiconductor package according to claim 1 wherein said conductive structure is coupled to said chip carrier using an electrically insulative adhesive material.
6. (Original) The semiconductor package according to claim 1 wherein said conductive structure is coupled to said chip carrier using a thermally conductive adhesive material.
7. (Original) The semiconductor package according to claim 1 wherein said conductive structure comprises a spring.

8. (Original) The semiconductor package according to claim 1 wherein said conductive structure comprises a block.
9. (Previously Presented) The semiconductor package according to claim 1 wherein said conductive structure comprises a surface mount technology (SMT) discrete component.
10. (Previously Presented) The semiconductor package according to claim 1 wherein a solder couples said conductive structure to said grounded pad;  
an electrically conductive adhesive material couples said conductive structure to said conductive lid; and  
an electrically insulative adhesive material couples said conductive structure to said chip carrier.
11. (Original) The semiconductor package according to claim 10 wherein said conductive structure comprises a conductive spring.
12. (Original) The semiconductor package according to claim 10 wherein said conductive structure comprises a block.
13. (Original) The semiconductor package according to claim 10 wherein said conductive structure comprises a surface mount technology (SMT) discrete component.

Claims 14 – 21 (Cancelled)

22. (Previously Presented) The semiconductor package of claim 1 wherein an end of said conductive lid extends beyond at least one side of said semiconductor chip.
23. (Previously Presented) The semiconductor package of claim 1 wherein said conductive structure is located on said first side of said chip carrier.

---

### **Remarks**

Applicants respectfully request entry of the amendment to claim 1 and cancellation of claims 14-21 as set forth herein to place the present application in condition for allowance or in better condition for purposes of appeal. Applicants respectfully request that claim 1 be amended to include the limitation of previously presented claim 21. No new matter has been added to the application by virtue of the present amendments. Applicants believe the present amendments do not raise new issues requiring further search by the Examiner.

### **Claim Rejections - 35 U.S.C. § 112**

The Examiner rejected claims 1 and 21 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 1 and 21 recited the limitation of “a conductive lid substantially coplanar with said first side of said chip carrier.” The Examiner indicated that this is confusing since the instant invention shows that the conductive lid is formed on top of the chip, and therefore, cannot be coplanar with said first side of said chip carrier.

Applicants respectfully request that independent claim 1 be amended to recite the limitation of previously presented claim 21 of “...a conductive lid thermally coupled to said semiconductor chip, wherein the entire length of said conductive lid is substantially parallel with said first side of said chip carrier;...”. Appropriate correction has been made to amended claim 1 in that the term “coplanar” has been replaced with “parallel”.

Applicants have canceled dependent claim 21.

Support for Applicants' amendments can be found, for example, in Fig. 4.

therefore, overcomes the examiner's rejection under 35 U.S.C. § 112, second paragraph.

**Claim Rejections - 35 U.S.C. § 102(e)**

The Examiner rejected claims 1 and 21-23 under 35 U.S.C. § 102(e), as being anticipated by Huang et al., U.S. Patent No. 6,472,743, hereinafter Huang. With regard to independent claim 1, the Examiner indicated that Huang discloses a semiconductor package incorporating the elements claimed by Applicants. The Examiner stated that Fig. 1 of Huang shows a chip carrier including ground pad, a semiconductor chip, a conductive lid, and a conductive structure. Applicants respectfully traverse the rejection under 35 U.S.C. § 102(e), and submit that Huang does not anticipate or suggest applicants' independent claim 1, as amended.

Huang does not anticipate or suggest Applicants' independent claim 1, as amended, or claims dependent thereupon. In Applicants' present application the conductive lid is thermally coupled, [170] in Applicants' Fig 4, to the semiconductor chip. Whereas, in the Huang patent there is neither mention nor implication whatsoever of such thermal coupling. In the Huang patent there is in fact a space between the semiconductor chip and the conductive lid (heat sink). This space is filled with an encapsulant, which is a conventional epoxy resin material (col. 6, lines 1-2), and as disclosed in the Huang patent (col. 6, lines 50-53) is poor in thermal activity. This is clearly inapposite to Applicants' present invention in which the conductive lid and semiconductor chip are directly thermally coupled to one another.

Additionally, in the Huang patent the Examiner indicates that Huang's use of solder balls [230] as shown in Fig. 1 of Huang, anticipates Applicant's conductive structure [400] as shown in Fig. 4 of the present application. An aspect of Applicants' invention is the use of blocks or pieces of metal (i.e., the conductive structures) that resemble and can be handled like discrete SMT components with the current SMT infrastructure of placement and joining. This allows the use of a flat lid, for example, without the complications, such as those that are the subject matter, and addressed by the Huang patent (i.e., mold flashing). The Huang patent does not use such SMT like structures, but rather uses solder balls, which are not analogous in either form nor function to that

of Applicants' use of conductive structures as shown and described in the present application.

Also, in the Huang patent the conductive lid (heat sink) is directly attached to the solder balls as shown in Fig. 1 of the Huang patent. With a direct attachment as shown and described in the Huang patent there are several disadvantages including the solder does not perform well as a stress buffer. That is, when solder is used, cracks or delaminations may be caused at the interface between the lid and the chip carrier due to thermal stresses. Such cracks can degrade the heat removal capacity of the package and further degrade electrical performance of the chip. In the present application the conductive lid is electrically coupled [410] in Applicants' Fig. 4, to the conductive structure rather than being directly attached as in the Huang patent. Thus, resolving the disadvantages listed above, as an electrically conductive silicone based adhesive material is used, which provides a better mechanical buffer for reducing stress between the conductive lid and the conductive structure.

Further, the semiconductor package disclosed in the Huang patent uses an encapsulant to fill all the cavities of the chip package. In the current application only the cavity formed between the semiconductor chip and chip carrier is underfilled with an epoxy for the purpose of reinforcing the semiconductor chip to chip carrier electrical interconnection.

Claims 21-23 are dependent upon Claim 1; and as discussed above, Claim 1, as amended, is not anticipated by Huang because Huang does not disclose all the elements of claim 1, as amended. Therefore, Applicants respectfully submit that the rejection of Claims 1 and 21-23 under 35 U.S.C. 102(e) in view of Huang has been overcome and it is respectfully requested that the pending claims be passed to issuance in view of the remarks.

The Examiner rejected claims 1, 8 and 21-23 under 35 U.S.C. § 102(e), as being anticipated by Shim et al., U.S. Patent No. 6,775,140, hereinafter Shim. With regard to independent claim 1, the Examiner indicated that Shim discloses a semiconductor package incorporating the elements claimed by Applicants. The Examiner stated that Fig. 8 of Shim shows a chip carrier including ground pad, a semiconductor chip, a conductive lid, and a conductive structure. Applicants

respectfully traverse the rejection under 35 U.S.C. § 102(e), and submit that Shim does not anticipate or suggest applicants' independent claim 1.

Applicants have amended independent claim 1 to recite the limitations of previously presented claim 21 of "...a conductive lid thermally coupled to said semiconductor chip, wherein the entire length of said conductive lid is substantially parallel with said first side of said chip carrier;...".

Applicants have canceled dependent claim 21.

Support for Applicants' amendments can be found, for example, in Fig. 4.

Shim does not anticipate or suggest Applicants' independent claim 1, as amended, or claims dependent thereupon. The Shim patent discloses an elaborately formed lid with many bends and openings, e.g. Fig. 8 of Shim patent. In contrast Applicants' present application does not disclose such an elaborate and complex lid, rather Applicants' application discloses a lid that is substantially planar and its entire length is parallel with the first side of the chip carrier. The use of such a planar conductive lid as described in the present application offers a number of advantages not afforded or possible with the elaborately formed lid as shown and described in the Shim patent. A conductive lid substantially planar and substantial parallel with the top surface of the chip carrier is less costly and is extendable to use for a number of different parts. Use of existing manufacturing equipment, such as the current SMT infrastructure, can be employed to attach the chip elements without requiring retooling or modification to the existing equipment.

Additionally, an aspect of Applicants' invention is the use of blocks or pieces of metal (i.e., the conductive structures), [108] in Applicant's Fig. 4, that resemble and can be handled like discrete SMT components with the current SMT infrastructure of placement and joining. This allows the use of a flat lid, for example, which as explained has a number of advantages. Further, the blocks act to bridge the physical gap between the conductive lid and the chip carrier, thus providing not only electrical and thermal contact but structural support as well. The Shim patent

does not use such conductive structures as those shown and described in Applicants' application, in fact in Shim the lid has to have protrusion extending downward to reach what the examiner has described as conductive structures [304, 306] in Shim's Fig. 8.

Further, Applicants' claim 1, as amended, includes the limitation of "...a conductive structure electrically coupled to said grounded pad and to said conductive lid; ..." In Shim; however, the only mention of electrical grounding of the conductive lid is found in Shim is "In addition to support the heat transfer functions, the contact pads 308 also enable direct electrical contact to substrate ground pads." (Column 8, lines 10-12). However, in Shim no detail is provided on how to accomplish the electrical connection. At most, implicit with the words above is a "dry contact" as opposed to electrical contact by using solder or an electrically conductive adhesive, as is shown and described in the present application. In Shim, preceding the mention of electrical contact (Column 8, lines 10-12), detail is provided about the thermal interface materials between the heat spreader and chip and between protrusion pads and the substrate (Col 7, lines 47-65). Consistency in writing would demand similar detail on how to accomplish the electrical contact. At best, "dry" electrical contact is implied. However, dry electrical contact would not be reliable in such a structure. During curing of the adhesive that is placed between protrusion pads and the substrate, expansion is likely as well as substrate warpage, especially for organic substrates. It is likely that the contact pads will not make a reliable electrical connection after the cure process. To accomplish a reliable electrical connection, a compressive normal force would be required. No description is provided on how the normal force would be achieved. Further, no description is provided on what metallurgy is needed to achieve a reliable electrical connection.

Claims 8 and 21-23 are dependent upon Claim 1, as amended; and as discussed above, Claim 1, as amended, is not anticipated by Shim because Shim does not disclose all the elements of claim 1, as amended.

In addition, with regards to claim 8, an aspect of Applicants' invention is the use of "blocks" or pieces of metal that can be handled with current SMT infrastructure of placement and joining. This allows the use of a flat lid, which is much less expensive than the elaborately formed



lid in the Shim patent. The blocks function to bridge the vertical space between the flat lid and substrate (about one mm) to accomplish electrical grounding, thus the use of the "discrete-like" conductive elements (blocks), which bridge most of the gap and allow the use of solder and electrically conductive adhesive to bridge smaller gaps such as 0.1 mm. Examiner references in Shim, col 6, lines 25-30 and links this to "block" which is the word Applicants use to describe a discrete-like SMT component. Applicants believe the examiner is in error in making this link. The Shim reference is describing a geometric feature (shape), such as a square that can be stamped and used as an orientation or alignment check to ensure that the lid is placed on the substrate correctly. Shim does not use "blocks" but rather "shape" to distinguish a correct orientation.

Therefore, Applicants respectfully submit that the rejection of Claims 1, 8 and 21-23 under 35 U.S.C §102(e) in view of Shim has been overcome and it is respectfully requested that the pending claims be passed to issuance in view of the amendments and remarks.

#### **Claim Rejections - 35 U.S.C. § 103(a)**

The Office Action stated that claims 2-4 are rejected under 35 U.S.C. § 103(a), as being unpatentable over Shim in view of U.S. Patent No. 6,225,694 issued to Terui. The Examiner rejected claim 5-6, 10 and 12 under 35 U.S.C. § 103(a), as being unpatentable over Shim and Terui as applied to claim 1 above, and further in view of U.S. Patent No. 5,866,943 issued to Mertol. The Examiner also rejected claim 7 under 35 U.S.C. § 103(a), as being unpatentable over Shim and Terui as applied to claim 1 above, and further in view of U.S. Patent No. 6,562,655 issued to Glenn et al. Examiner also rejected claim 9 under 35 U.S.C. § 103(a), as being unpatentable over Shim and Terui as applied to claim 1 above, and further in view of U.S. Patent No. 6,630,661 issued to Hoffman. Examiner also rejected claim 11 under 35 U.S.C. § 103(a), as being unpatentable over Shim, Terui and Mertol as applied to claim 10 above, and further in view of Glenn. Examiner further rejected claim 13 under 35 U.S.C. § 103(a), as being unpatentable over Shim, Terui and Mertol as applied to claim 1 above, and further in view of Hoffman.

As discussed above, Applicants respectfully submit that Shim, individually or in

combination with Terui, Mertol, Glenn, and/or Hoffman, do not teach or suggest Applicants' independent claim 1, as amended, or any claims dependent thereupon.

Based on the foregoing, Applicants respectfully traverse the rejection under 35 U.S.C. § 103(a) and submit that the rejections to claims 2-7 and 9-13 have been overcome.

### **Conclusion**

In light of the foregoing remarks, all of the claims now presented are believed to be in condition for allowance, and Applicants respectfully request that the outstanding rejections be withdrawn and this application be passed to issue at an early date.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application. No fee is due by virtue of this response. However, if the PTO determines that a fee is required, please charge Applicants' Deposit Account, 09-0456.

Respectfully submitted,  
For: Michael Gaynes, et al.

By:       /Ryan Simmons/        
Ryan K. Simmons  
Registration No. 45,848  
Telephone No.: (802) 769-1809  
Fax No.: (802) 769-8938  
EMAIL: rksimmon@us.ibm.com

International Business Machines Corporation  
Intellectual Property Law - Mail 972E  
1000 River Road  
Essex Junction, VT 05452